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EXAMINER	
YUEN, KAN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,296	KINSTLER, GARY A.	
	Examiner	Art Unit	
	KAN YUEN	2464	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/16/2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11,15-20 and 37-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11,15-20 and 37-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see remark pages, filed on 7/16/2010, with respect to the rejection(s) of claim(s) 7-11, 15-20 and 37-46 under 103 Rejections have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Alkalai et al. (Pat No.: 7020076).

Claim Rejections - 35 USC § 103

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 9, 11, 37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alkalai et al. (Pat No.: 7020076) in view of Baretzki (Pat No.: 7707281).

For claim 37, Alkalai et al. disclosed the method of clearing latch-up and other single event functional interrupts in a data processing system having a plurality of nodes operatively connected to a serial data bus, the method comprising:

periodically transmitting a first message from a first node to a second node on a first line of the serial data bus (Alkalai et al. see column 12, lines 1-20. The controlling master (root/source node) periodically sends a "fail silence" message to all I2C nodes). The fail silence message is broadly interpreted to be the first message;

determining whether the first message was received by the second node (Alkalai et al. see column 12, lines 1-35. If one of the nodes is babbling so that the fail silence message is blocked or delayed, the I2C bus fail-silence timer of each node will time out... At this time, another timer in the controlling master node will un-mute the node itself and send a message to re-enable the other nodes individually. If a node causes the bus fail again while it is enabled, it will be identified as the failed node. When a node or one of its links fails in the non-responsive mode, it will not be able to respond to requests and messages will not be able to pass through the node. The existence of the failure can easily be detected by the bus timeout, message re-transmission, heartbeat or polling); and

transmitting a recovery command to the second node if the second node does not respond to the first message, the recovery command transmitted, the recovery command causing the second node to disrupt a mono-stable condition in the second node and restore functionality of the second node without disrupting the first node and any other nodes of the plurality (Alkalai et al. see column 12, lines 29-65. After the failed

node is identified, the root node will first interrogate the health of the nearest non-responsive node (target node) through the I2C bus. Similarly, if a node in the I2C bus becomes non-responsive, the root node can interrogate the health of the non-responsive node through the IEEE 1394 bus, and command the non-responsive node to reset its I2C bus interface). In other words, after the non-responsive node is being identified, the root node will interrogate the non-responsive node by transmitting a command (recovery command) to the non-responsive node to instruct the node to clear its non-responsive (mono-stable) condition by resetting its interface so that original functionality can be restored. Since the term mono-stable is not specifically define, the Examiner broadly interprets the non-responsive node is experiencing a mono-stable condition. Thus, the command is only being sent to the non-responsive node without disrupting any other nodes in the system. By using the technique, the system can continue to operate, in the presence of faults, to meet the system specification without failure of the entire system (see column 1, lines 50-60).

However, Alkalai et al. did not explicitly disclose the feature of transmitting a recovery command to the second node via an alternative data bus.

Baretzki from the same or similar fields of endeavor disclosed the feature of transmitting a recovery command to the second node via an alternative data bus (Baretzki column 3, lines 45-57, and see fig. 1. This second situation must however be handled since it dangerously prejudices the operational reliability. To deal with this problem, a standby bus 6 is connected between the two routers, which enable a reset (recovery) command to be sent).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method as disclosed by Alkalai et al. and to include the feature as disclosed by Baretzki.

The motivation would be to improve redundancy in the network.

Regarding claim 7, Alkalai et al. disclosed the feature wherein the nodes transmit a plurality of messages in each of a plurality of frames on the first line of the serial data bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame (Alkalai et al. see column 12, lines 1-20. The controlling master (root/source node) periodically sends a "fail silence" message to all I2C nodes). The fail silence message is broadly interpreted to be the first message. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 9, Alkalai et al. disclosed the feature wherein determining whether the first message was received includes waiting for a reply from the second node (Alkalai et al. see column 12, lines 1-20).

Regarding claim 11, Baretzki disclosed the feature wherein the second bus is a different type of bus than the serial data bus (Baretzki column 3, lines 45-57, and see fig. 1. This second situation must however be handled since it dangerously prejudices the operational reliability. To deal with this problem, a standby bus 6 is connected between the two routers, which enables a reset (recovery) command to be sent, in other words a command sent by the slave to suspend the master's port 3).

Regarding claim 40, Alkalai et al. disclosed the feature wherein the recovery command causes a bus interface circuit operatively connecting the second node to the first bus to be re- initialized (Alkalai et al. see column 12, lines 29-65. After the failed node is identified, the root node will first interrogate the health of the nearest non-responsive node (target node) through the I2C bus. Similarly, if a node in the I2C bus becomes non-responsive, the root node can interrogate the health of the non-responsive node through the IEEE 1394 bus, and command the non-responsive node to reset its I2C bus interface).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alkalai et al. (Pat No.: 7020076) in view of Baretzki (Pat No.: 7707281) as applied to claim 37 above, and further in view of Engels et al. (Pub No.: 2004/0213174).

Regarding claim 8, Alkalai et al. and Baretzki did not disclose the feature wherein the nodes transmit a plurality of messages in each of a plurality of frames on the first line of the serial data bus, the first message is at least one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once each minor frame.

Engels et al. from the same or similar fields of endeavor disclosed the feature wherein the nodes transmit a plurality of messages in each of a plurality of frames on the first line of the serial data bus, the first message is at least one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is

transmitted once each minor frame (Engels et al. see paragraph 0028, lines 1-4). The uplink frame, which includes plurality of mini time slot frames, is allocated for data transmission in each individual slot frame. The data can be any kind of messages.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method as disclosed in Alkalai et al. in view of Baretzki and to include the feature as disclosed by Engels et al.

The motivation for using the feature as taught by Engels et al. in the network of Kramer et al. Gupta et al. and Fuchs et al. being that the minor frames can be transmitted without major delay.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alkalai et al. (Pat No.: 7020076) in view of Baretzki (Pat No.: 7707281) as applied to claim 37 above, and further in view of Kim (Pat No.: 6064554).

For claim 10, Alkalai et al. and Baretzki did not disclose the feature of detecting a current surge in a bus interface circuit operatively connecting the second node to the first bus; and cycling power to the bus interface circuit in response to detecting the current surge in the bus interface circuit.

Kim et al. from the same or similar fields of endeavor disclosed the feature of detecting a current surge in a bus interface circuit operatively connecting the second node to the first bus; and cycling power to the bus interface circuit in response to

detecting the current surge in the bus interface circuit (Kim et al. see column 2, lines 13-40). The power unit is couple to the over-current or current surge detector.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method as disclosed by Alkalai et al. in view of Baretzki, to include the feature as disclosed by Kim.

The motivation for using the feature being that the over-current detection can provide protections to system cause by power outrage.

7. Claims 38 and 39 rejected under 35 U.S.C. 103(a) as being unpatentable over Alkalai et al. (Pat No.: 7020076) in view of Baretzki (Pat No.: 7707281) as applied to claim 37 above, and further in view of Kramer et al. (Pat No.: 6466539).

Regarding claim 38, Alkalai et al. and Baretzki did not explicitly disclose the feature wherein the second node includes a physical layer controller connected to the serial data bus and link layer controller and wherein a monostable condition is disrupted in at least one of the physical layer controller and the link layer controller.

Kramer from the same or similar fields of endeavor disclose the feature wherein the second node includes a physical layer controller connected (Kramer et al. control modules 56, 58 or 60, 62) to the serial data bus (busses 10, 12) and link layer controller (Kramer et al. control modules 56, 58 or 60, 62); and wherein a monostable condition is disrupted in at least one of the physical layer controller and the link layer controller

(Kramer et al. column 5, lines 10-67, column 6, lines 1-30). Both controller modules 56, 58 in subscriber 18 are monitoring each other for failure.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method as disclosed by Alkalai et al. in view of Baretzki and to include the feature as disclosed by Kramer.

The motivation would be to provide redundancy in the network.

Regarding claim 39, Kramer disclosed the feature wherein the link layer controller is coupled to and dc-isolated from the physical layer controller; and wherein disrupting a monostable condition in the link layer controller is independent of disrupting a monostable condition in the physical layer controller (Kramer et al. column 6, lines 1-35). The fault-proof comparator consists of the two homogenous units A0 and B0, the galvanically separated link 96 (isolated) such as an optical coupler and relays K1, K2. The relays have forced controller contacts, a property where the contacts for the two relay states, i.e. the normally open and the normally closed contacts cannot be opened or closed at the same time, thus they are independent.

8. Claims 16, 19, 20, 41 and 44-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alkalai et al. (Pat No.: 7020076) in view of Broseghini et al. (Pat No.: 5761489) and further in view of Baretzki (Pat No.: 7707281).

Regarding claim 41, Alkalai et al. disclosed a data processing system comprising:

a serial data bus including at least one line (Alkalai et al. fig. 1, IEEE 1394 bus 130 or I2C bus 140);

a plurality of nodes operatively connected to the serial data bus, each node including a bus interface connected to the serial data bus (Alkalai et al. fig. 1, node devices 110, see column 3, lines 30-47, column 6 lines 1-25, Fig. 1 shows an avionic system 100 that comprises node devices 110 and non-node devices 120. At the system level, the node devices 110 are interconnected by the fault-tolerant buses, each of which includes an IEEE 1394 bus 130 and an I2C bus 140);

wherein at least one of the nodes periodically transmits a first message on a first line of the serial data bus to other nodes (Alkalai et al. see column 12, lines 1-20. The controlling master (root/source node) periodically sends a "fail silence" message to all I2C nodes). The fail silence message is broadly interpreted to be the first message;

transmits a recovery command to a node that does not respond to the first message; wherein the non-responding node receives the recovery command and, in response restores correct operation, including disrupting a mono-stable condition (Alkalai et al. see column 12, lines 29-65. After the failed node is identified, the root node will first interrogate the health of the nearest non-responsive node (target node) through the I2C bus. Similarly, if a node in the I2C bus becomes non-responsive, the root node can interrogate the health of the non-responsive node through the IEEE 1394 bus, and command the non-responsive node to reset its I2C bus interface). In other words, after the non-responsive node is being identified, the root node will interrogate the non-responsive node by transmitting a command (recovery command) to the non-

responsive node to instruct the node to clear its non-responsive (mono-stable) condition by resetting its interface so that original functionality can be restored;

However, Alkalai et al. did not explicitly disclose the features wherein the non-responding node receives the recovery command and, in response, clears a latch-up; and the recovery command transmitted via a second line of the serial bus or by a second data bus.

Broseghini et al. from the same or similar fields of endeavor disclosed the feature wherein the non-responding node receives the recovery command and, in response, clears a latch-up (Broseghini et al. see fig. 2, column 7, lines 25-35. Test Reset signal 78 is asserted in order to clear the latches 62 and 63 in modules 36 and 38).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system as disclosed by Alkalai et al. to include the feature as disclosed by Broseghini et al.

The motivation would be to provide fault recovery in the system.

Baretzki from the same or similar fields of endeavor disclosed the feature wherein the recovery command is transmitted via a second line of the serial bus or by a second data bus (Baretzki column 3, lines 45-57, and see fig. 1. This second situation must however be handled since it dangerously prejudices the operational reliability. To deal with this problem, a standby bus 6 is connected between the two routers, which enable a reset (recovery) command to be sent).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system as disclosed by Alkalai et al. in view of Broseghini et al. to include the feature as disclosed by Baretzki.

The motivation would be to provide reliability in the network.

Regarding claim 16, Alkalai et al. disclosed the feature wherein the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame (Alkalai et al. see column 12, lines 1-20. The controlling master (root/source node) periodically sends a "fail silence" message to all I2C nodes). The fail silence message is broadly interpreted to be the first message. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 19, Baretzki disclosed the feature wherein the second bus is a different type of bus than the first bus (Baretzki column 3, lines 45-57, and see fig. 1. This second situation must however be handled since it dangerously prejudices the operational reliability. To deal with this problem, a standby bus 6 is connected between the two routers, which enables a reset (recovery) command to be sent, in other words a command sent by the slave to suspend the master's port 3).

Regarding claim 20, Alkalai et al. disclosed the feature wherein the nodes include a bus interface circuit operatively connected to the serial data bus; and means for receiving the recovery command on the second bus and for re-initializing the bus interface circuit in response to the command (Alkalai et al. see column 12, lines 29-65.

After the failed node is identified, the root node will first interrogate the health of the nearest non-responsive node (target node) through the I2C bus. Similarly, if a node in the I2C bus becomes non-responsive, the root node can interrogate the health of the non-responsive node through the IEEE 1394 bus, and command the non-responsive node to reset its I2C bus interface).

Regarding claim 44, Alkalai et al. disclosed the feature wherein each node further include a watchdog timer for monitoring its bus interface (Alkalai et al. see column 11, lines 20-25).

Regarding claim 45, Broseghini et al. disclosed the feature wherein clearing the latch-up and restoring correct operation includes turning off and then turning back on the bus interface, and also reinitializing affected bus circuitry (Broseghini et al. see fig. 2, column 7, lines 25-35. Test Reset signal 78 is asserted in order to clear the latches 62 and 63 in modules 36 and 38).

Regarding claim 46, Alkalai et al. disclosed the feature wherein the bus interface is not radiation- hardened (Alkalai et al. see column 6, lines 1-25).

9. Claims 15, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alkalai et al. (Pat No.: 7020076) in view of Baretzki (Pat No.: 7707281) and Broseghini et al. (Pat No.: 5761489) as applied to claim 41 above, and further in view of Kim (Pat No.: 6064554).

Regarding claim 15, Alkalai et al., Baretzki and Broseghini et al. did not explicitly disclose the feature wherein the nodes further detect a current surge in the bus

interface and report the current surge in the bus interface circuit to the node sending the first message.

Kim et al. from the same or similar fields of endeavor disclosed the feature of detecting a current surge in a bus interface circuit operatively connecting the second node to the first bus; and cycling power to the bus interface circuit in response to detecting the current surge in the bus interface circuit (Kim et al. see column 2, lines 13-40). The power unit is couple to the over-current or current surge detector.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system as disclosed by Alkalai et al. in view of Broseghini et al. and Baretzki, to include the feature as disclosed by Kim.

The motivation for using the feature being that the over-current detection can provide protections to system caused by power outrage.

Regarding claim 18, Kim disclosed the feature wherein each node includes a bus interface circuit operatively connected to the serial data bus; means for detecting a current surge in the bus interface circuit; and means for cycling power to the bus interface circuit in response to detecting the current surge (Kim et al. see column 2, lines 13-40). The power unit is couple to the over-current or current surge detector.

10. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alkalai et al. (Pat No.: 7020076) in view of Broseghini et al. (Pat No.: 5761489) and Baretzki

(Pat No.: 7707281) as applied to claim 41 above, and further in view of Engels et al. (Pub No.: 2004/0213174).

Regarding claim 17, Alkalai et al., Broseghini et al. and Baretzki did not disclose the feature wherein the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once in each minor frame.

Engels et al. from the same or similar fields of endeavor disclosed the feature wherein the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once in each minor frame (Engels et al. see paragraph 0028, lines 1-4). The uplink frame, which includes plurality of mini time slot frames, is allocated for data transmission in each individual slot frame. The data can be any kind of messages.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method as disclosed in Alkalai et al. in view of Broseghini et al. and Baretzki, to include the feature as disclosed by Engels et al.

The motivation for using the feature being that the minor frames can be transmitted without major delay.

11. Claims 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alkalai et al. (Pat No.: 7020076) in view of Broseghini et al. (Pat No.: 5761489) and

Baretzki (Pat No.: 7707281) as applied to claim 37 above, and further in view of Kramer et al. (Pat No.: 6466539).

Regarding claim 42, Alkalai et al., Broseghini et al. and Baretzki did not explicitly disclose the feature wherein the bus interface includes a physical layer controller that is connected to the serial data bus, and a link layer controller that is coupled to and galvanically isolated from the physical layer controller, and wherein a monostable condition in the link layer controller is disrupted independently of a monostable condition in the physical layer controller.

Kramer et al. from the same or similar fields of endeavor disclosed the feature wherein the bus interface includes a physical layer controller that is connected to the serial data bus, and a link layer controller that is coupled to and galvanically isolated from the physical layer controller, and wherein a monostable condition in the link layer controller is disrupted independently of a monostable condition in the physical layer controller (Kramer et al. column 6, lines 1-35). The fault-proof comparator consists of the two homogenous units A0 and B0, the galvanically separated link 96 such as an optical coupler and relays K1, K2 and controls an output level, in which the power supply of the relevant device is located and which will interrupt the power supply in case the comparator gives the relevant signal, so that the device can be rendered safe. The relays have forced controller contacts, a property where the contacts for the two relay states, i.e. the normally open and the normally closed contacts cannot be opened or closed at the same time, thus they are independent.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method as disclosed by Alkalai et al. in view of Broseghini et al. and Baretzki and to include the feature as disclosed by Kramer.

The motivation would be to provide redundancy in the network.

Regarding claim 43, Kramer et al. disclosed the feature wherein each node further includes a second data bus and means for coupling the link layer controller to the second data bus, the means also dc-isolating the link layer controller from the second data bus (Kramer et al. column 6, lines 1-35).

Examiner's Note:

Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAN YUEN whose telephone number is (571)270-1413. The examiner can normally be reached on Monday-Friday 10:00a.m-3:00p.m EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky O. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kan Yuen/
Examiner, Art Unit 2464

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2464

KY